PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Inventor: Thomas Grassl

Application No.: 09/926,377
Confirmation No: 9840

Filed: December 13, 2001

Attorney No.: GRAS3003/JEK
Customer No.: 23364

Examiner: David L. Hogans

Art Unit: 2813

For: CIRCUIT SUITABLE FOR VERTICAL INTEGRATION AND METHOD OF PRODUCING SAME

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This appeal brief is filed pursuant to the appellants' appeal to the Board of Patent Appeals and Interferences from the final rejection of the claims in the above-application.

I. REAL PARTY OF INTEREST

The real party in interest is the assignee of record: Giesecke & Devrient GmBH (Munich, GERMANY).

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 19-26 are currently pending in the above-referenced application.

Claims 1-18 have been canceled.

Claims 25-26 are deemed allowable.

Claims 19-21, and 23 presently stand rejected.

Applicants appeal from the rejection of claims 19-21, and 23. Claims 20-21 depend from claim 19.

A copy of appealed claims 19-21, and 23 are included in the attached Appendix I.

IV. STATUS OF AMENDMENTS

An amendment was filed on February 1, 2005. In the amendment claims 24 and 26 are amended to correct a minor informality.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In each of the appealed claims, methods are generally provided for improving known procedures for producing vertical electrical connections. In particular, the methods are directed to forming vertically integratable circuits produced by planar technology which are disposed vertically on top of each other resulting in three-dimensional circuits (see FIGs. 1-2; page 1, lines 1-12; page 2, lines 8-17). The claims are directed to improvements for making these vertically integratable circuits which minimize the manufacturing steps to increased production yield (page 2, lines 12-21). For the claimed invention, vertical electrical contacts are produced during the actual manufacture of the vertically integratable circuit itself instead of waiting for a finished substrate to start making electrical contacts which simplifies and improves the production process (page 2, lines 8-17).

Each of the appealed claims recites an improvement over known methods for producing vertically integratable circuits. This allows the formation of electrical connections during the actual layering of the circuit to reduce manufacturing steps and improve yield. The claimed improvement includes initially providing a first and second substrate with a first insulating layer arranged inbetween. Active circuit components are then provided within the first (top) substrate via gaps formed in the top substrate to form a first circuit layer (see FIGs. 1a-1b; page 2, lines 26-30; page 3, lines 1-9). Thereafter, a second insulating layer is formed above the first circuit layer and gaps are formed in this layer that extend into the first circuit layer to communicate with the active circuit components thereon (see FIGs. 1c-1d; page 3, lines 16-23).

After the second insulating layer and gaps therein are formed, the gaps are filled with a first metalization to form first vertical contacts with the first circuit layer (see FIG. 1e; page 3, lines 24-28). Thereafter, the second substrate layer is thinned to expose the first insulating layer and gaps are formed in this layer that extend to the first vertical contact via the first circuit layer to communicate with the active circuit components thereon (see FIGs. 1f-1g; page 4, lines 5-19).

After the gaps are formed in the first insulating layer, the gaps are filled with a second metalization to form second vertical contacts with the first vertical contact to communicate with the first circuit layer and active circuit components thereon (see FIGs. 1h; page 4, lines 20-27).

Claims 20-21 recite additional features relating to an improved method for producing a vertically integratable circuit. Claim 20 further describes that the second metalization, via the gaps in the first insulating layer, are interrupted at the locations corresponding to the first vertical contact (see FIG. 1h), and Claim 21 further recites that active circuit components of the first circuit layer surround the connection between the first and second vertical contacts (see FIG. 1h).

Claim 23 recites a vertically integratable circuit having similar features to those recited in Claim 19.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 19, 21, and 23 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,426,072 (Finnila). Claims 19 and 23 stand finally rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,104,081 (Dekker et al. – "Dekker"). And Claim 20 stands finally rejected under 35 U.S.C. § 103(a) as being obvious over Finnila and U.S. Patent 6,495,454 (Livengood et al. – "Livengood").

Copies of the relevant patents are included in the attached Appendix II, and a copy of the final rejection dated September 3, 2004 is attached as Appendix III.

VII. ARGUMENT

A. Overview

Regarding the § 102 rejections, both Finnila and Dekker fail to disclose or suggest each and every feature, whether expressly or inherently, recited in claims 19-21, and 23 of the pending application.

Also, regarding the § 103 rejection, Finnila and Livengood, either alone or in combination, fail to disclose or suggest each and every feature, whether expressly or inherently, recited in claim 20 of the pending application.

B. Pertinent Law

1. Anticipation

To establish anticipation under 35 U.S.C. § 102, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Vergegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). There is no anticipation "unless all of the same elements are found in exactly the same situation and united in the same way ... in a single prior art reference." *Perkin-Elmer Corp. v. Computervision Corp.,* 732 F.2d 888, 894, 221 USPQ 669, 673 (Fed. Cir. 1984) (citing *Kalman v. Kimberly-Clark Corp.,* 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983). Absence from the reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible, Inc.,* 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed.Cir.1986).

2. Obviousness

To establish obviousness under 35 U.S.C. § 103(a), differences between the subject matter sought to be patented and the prior art reference are such that the subject matter as a whole would have been obvious to one skilled in the art at the time of the invention. Accordingly, in making an assessment of differences, §103 specifically

requires consideration of the claimed invention as a whole guided by the accepted wisdom at the time the invention was made. *Ruiz v. A.B. Chance Co.,* 357 F.3d 1270, 1275, 69 U.S.P.Q.2d (BNA) 1686, 1689 (Fed. Cir. 2004).

Identification of each element of a claimed invention in prior art references is insufficient to defeat patentability of the whole claimed invention. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d (BNA) 1453, 1457 (Fed. Cir. 1998). Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching to select and combine the references relied on as evidence of obviousness. *In re Lee,* 277 F.3d 1338, 1342-43, 61 U.S.P.Q.2d (BNA) 1430, 1433 (Fed. Cir. 2002) (citing *McGinley v. Franklin Sports, Inc.,* 262 F.3d 1339, 1351-52, 60 U.S.P.Q.2d 1001 (BNA), 1008 (Fed. Cir. 2001)).

In making a rejection based on obviousness, particular findings and specific reasons must be provided as to why a skilled artisan would have been motivated to select references and to combine them to render a claimed invention obvious. *See In re Kotzab,* 217 F.3d 1365, 1371, 55 U.S.P.Q.2d (BNA) 1313, 1317 (Fed. Cir. 2000); *See also In re Rouffet,* 149 F.3d at 1359, 47 U.S.P.Q.2d (BNA) at 1459 (Fed. Cir. 1998).

Evidence of the motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d (BNA) 1614, 1617 (Fed. Cir. 1999). Whether an express or implicit showing is relied upon, particular findings related thereto must be provided therewith. Id. When general knowledge is relied upon to negate patentability, that knowledge must be articulated in the record and cannot be resolved on "subjective belief and unknown authority." *Lee*, 277 F.3d at 1342-1345, 61 U.S.P.Q.2d (BNA) at 1433-35.

C. Basic Description of the Finnila Patent

The Finnila Patent describes a method for manufacturing a three-dimensional integrated circuit from stacked silicon-on-insulator (SOI) wafers using a temporary silicon substrate (see Abstract; FIGs. 1-6). Particularly, Finnila describes initially providing an SOI wafer including a silicon film 12 separated from a bulk silicon substrate 10 by an insulating layer 11 (see FIG. 1; col. 3, lines 4-6). Thereafter, insulating regions 13 are formed on the surface of the top silicon film layer 12, and then trenches 14 are formed to define feedthroughs 16 in both the insulating regions 13 and the top silicon layer 12 that extend to the insulating layer 11 (see FIGs. 2-3; col. 3, lines 45-55).

After formation of the trenches 14, the trench walls are oxidized to form a temporary insulating layer 15 within the trenches and extending over the upper surface of the top silicon film 12 (see FIG. 4; col. 3, lines 56-63). Thereafter, further processing occurs to form an integrated circuit where the temporary insulating layer 15 is removed, and another insulating layer 17 is formed on the silicon film 12 with gate electrodes 18 deposited thereon (see FIG. 5; col. 4, lines 18-29). Also, p+ and n+ regions are formed within silicon film 12, and another insulating layer 20 is deposited over gate electrodes 18. Thereafter, openings are defined within the insulating layer 20 and metalization 21 is deposited within the feedthroughs 16 to contact the electrodes 18 deposited on insulating layer 17 and the p+, n+ regions within silicon film 12 to form a number of active devices (see FIG. 5; col. 4, lines 29-40).

Further, the bottomside silicon substrate 10 is removed and openings are formed in the now exposed insulating layer 1 extending to the feedthroughs 16 and metalization 21. Then, bonding pads 28, an overglass layer 29, and indium bumps 30 are formed within and over the openings to produce a circuit assembly having active electrical components located within the silicon layer 12, and topside and bottomside interconnects for coupling to other devices. Further, bottomside metalization 31 may be added to provide interconnection between the bonding pad 28 and indium bump 30 allowing flexibility in locating the bumps (see FIG. 6; col. 5, lines 10-54).

D. Basic Description of the Dekker Patent

The Dekker Patent describes a method for manufacturing a semiconductor device with semiconductor elements formed in a layer of semiconductor material glued on a support wafer (see Abstract; FIGs. 1-6). Particularly, Dekker describes initially providing a semiconductor wafer 1 including a top layer of semiconductor material 4 disposed on an insulating layer 3 (see FIG. 1; col. 3, lines 24-29). Thereafter, field effect transistors (FET) are created using p-type doping elements 5 formed within top semiconductor layer 4, each FET including a gate electrode 8, source 9, and drain 10 where the FET is covered with an insulating layer 11 (see FIGs. 2-3; col. 3, lines 39-47).

After forming the insulating layer 11, contact windows 12 are provided therein which extend to each FET and the insulating layer 3, and conductor tracks 14 are formed in each contact window 12 (see FIG 4; col. 3, lines 48-50). Further, the bottomside material 18 of semiconductor wafer 1 is removed, exposing the insulating layer 3, and contact windows 19, including conductive elements 20, each formed from the topside of the wafer 1 are provided therein which extend to the source 9 of each FET (see FIG. 5; col. 3, lines 66-67; col. 4, lines 1-11). Then, a contact wire 21 is provided that is bonded to the conductive elements to provide a connection with each FET to produce the semiconductor device (see FIG. 6; col. 4, lines 12-25).

E. Basic Description of the Livengood Patent

The Livengood Patent describes a structure for interconnecting circuits for power distribution in semiconductor devices (see Abstract; FIGs. 1-4). Particularly, Livengood describes a backside interconnect structure to deliver power through the substrate to the front side of an integrated circuit.

F. The Subject Matter Recited in Claims 19-21, and 23 is Not Anticipated by the Finnila Patent

In the discussion that follows, the appellants submit that the method of producing a vertically integratable circuit of claims 19-21, and the apparatus of claim 23 of the

pending application, respectively, differ from the teachings of the Finnila reference on the basis of the following particulars:

a) failure to disclose or suggest providing a first substrate with active circuit components along and within at least one portion thereof to define a first circuit layer;

b) failure to disclose applying a second insulation layer over a first circuit layer, and forming at least one first gap through the second insulation layer that extends at least a portion into the first circuit layer and is in communication with the active circuit components thereof; and

c) failure to disclose applying a second metalization along the second side of the first insulation layer, at least a portion of the second metalization extending through an at least one second gap to contact the first side vertical contact and defining a second side vertical contact as recited.

1. The Finnila patent fails to disclose or suggest providing a first substrate with active circuit components along and within at least one portion thereof to define a first circuit layer

In contrast to this recited feature of claims 19-21, Finnila expressly discloses providing a first substrate layer (top silicon layer 12) that is completely devoid of any active circuit components to define a first circuit layer. Particularly, Finnila provides an SOI wafer 1 solely composed of a bottomside bulk silicon wafer 10 separated from a topside silicon film 12 by an insulating layer 11 (see FIG. 1; col. 3, lines 4-17). Thereafter, insulating portions 13, 15, 17 are subsequently provided and gate electrodes 18 are then deposited on insulating layer 17, via feedthrough 16, to serve as the gate region for a transistor formed by the semiconductor device 1 (see FIGs. 2-5; col. 4, lines 18-34).

However, later building up insulating and electrical components on top of a first substrate is not equivalent to providing a first substrate with active circuit components to define a first circuit layer as recited. Finnila provides a first substrate 12 with no

additional components as it is simply a silicon layer provided on the other side of an insulating layer 11.

Essentially, Finnila teaches that all layers of the semiconductor device 1 which include bottom substrate 10, middle insulating layer 11, top substrate 12, and multiple insulating layers 13, 15, 17 must first be built up before any active circuit elements are provided within the first substrate 12. In contrast, the present invention claims a vertically integratable circuit that provides a first substrate with active circuit components to define a first circuit layer. There is a significant difference between having to build up multiple layers of silicon and insulating material before any formation of electrical connections can begin, as disclosed by Finnila, as opposed to simply providing one of the first layers of the device (the first substrate) with active circuit components to define a first circuit layer as recited.

Further, the first circuit layer (active circuit component) formed in Finnila is actually gate electrode 18 which is formed on top of first substrate 12 (see FIG. 5; col. 4, lines 28-30), but not along and within at least one portion thereof as recited. Depositing a circuit component on top of a first substrate to define a first circuit layer as disclosed by Finnila is not equivalent to the circuit component being along and within at least one portion of the first substrate to define a first circuit layer as recited.

The final rejection is premised on the erroneous observation of viewing the finished Finnila semiconductor device 1 (see FIG. 5) as a whole and noting its similarity with the present invention, without considering the critical, inventive steps towards vertically building up each particular layer of the integrated circuit where these individual, recited steps greatly differ from the steps taught or suggested by Finnila.

The final rejection fails to consider each individual step undertaken by the Finnila patent towards producing the semiconductor device, and comparing each individual step with the steps as recited towards producing a vertically integratable circuit. It is asserted that the Finnila patent fails to provide any active circuit components until all layers of the semiconductor device are built up, and then still fails to provide an active

circuit component (defining a first circuit layer) along and within at least one portion of a first substrate.

Thus, the Finnila patent fails to disclose or suggest providing a first substrate with active circuit components along and within at least one portion thereof to define a first circuit layer as recited in claims 19-21.

2. The Finnila patent fails to disclose or suggest applying a second insulation layer over a first circuit layer, and forming at least one first gap through the second insulation layer that extends at least a portion into the first circuit layer and is in communication with the active circuit components thereof

As contended above, Finnila does not provide a first substrate layer (top silicon layer 12) with any active circuit components to define a first circuit layer. After providing the top silicon layer 12, Finnila discloses forming insulating portions 13, feedthroughs 16 therein, and then another insulating portion 15 all over top silicon layer 12 (see FIGs. 1-4; col. 3, lines 45-63). Thus, Finnila provides insulating portions 13, 15 over a silicon layer 12 rather than a first circuit layer as recited.

Finnila builds up all non-electrical components of the semiconductor device (e.g., silicon layer 12, and insulating portions 13, 15) before any formation of circuit components including forming insulating layers 13, 15 over a silicon layer 12. There is a significant difference between having to build up multiple layers of silicon and insulating material before any formation of electrical connections can begin as disclosed by Finnila as opposed to simply providing one of the first layers of the device (the first substrate) with active circuit components to define a first circuit layer leading to applying an insulation layer over the circuit layer as recited.

Further, even if a first circuit layer can be found in Finnila, the second insulating elements 13, 15 formed in Finnila are actually insulating portions rather than insulation layers as recited (see FIGs. 3-4). Insulating elements 13, 15 formed in Finnila do not

cover the full length of underneath silicon layer 12, and therefore cannot be considered an actual insulation layer as recited, but rather are insulating portions that cover particular, partial portions of silicon layer 12. Providing an element to insulate a partial portion of an underneath layer, as disclosed by Finnila, is not equivalent to applying an insulation layer over a first circuit layer as recited.

Again, the final rejection is premised on the erroneous observation of viewing the finished Finnila semiconductor device 1 (see FIG. 5) as a whole and noting its similarity with the present invention. This appears to be done by the examiner without considering the critical, inventive steps of the pending application towards vertically building up each particular layer of the integrated circuit. Such individually recited steps greatly differ from the steps taught or suggested by Finnila.

The final rejection fails to consider each individual step undertaken by the Finnila patent towards producing the semiconductor device, and comparing each individual step with the steps as recited towards producing a vertically integratable circuit. It is asserted that the Finnila patent fails to provide any active circuit components until all layers of the semiconductor device are built up, and then still fails to provide an active circuit component (defining a first circuit layer) along and within at least one portion of a first substrate.

Therefore, the Finnila patent fails to disclose or suggest applying a second insulation layer over a first circuit layer, and forming at least one first gap through the second insulation layer that extends at least a portion into the first circuit layer and is in communication with the active circuit components thereof as recited in claims 19-21.

3. The Finnila patent fails to disclose or suggest applying a second metalization along the second side of the first insulation layer, wherein at least a portion of the second metalization extends through an at least one second gap to contact the first side vertical contact and defines a second side vertical contact.

In contrast to this recited feature of claims 19-21 (and equivalently recited in claim 23), Finnila expressly discloses providing bonding pads 28, an overglass layer 29, and bottomside indium bumps 30 to the second side of the first insulation layer 11 for contacting topside metalization 21 (see FIG. 6; col. 5, lines 31-54). Particularly, Finnila provides bonding pads 28 in the contact openings made in the first (underside) insulation layer 11 which protrude through the underside portion of the opening, overlays these protruding pads with the overglass layer 29, and forms the indium bumps 30 on top of the overglass (see FIG. 6; col. 5, lines 31-54). And optionally, metalization 31 may be provided outside of the contact openings, after formation of the bonding pads 28, to connect the pads with the overglass layer 29 to allow flexibility for positioning the indium bumps 30.

Finnila makes no mention of applying a second metalization extending through at least one second gap to contact a first side vertical contact as recited. Essentially, Finnila instead uses the bonding pads 28 within the second gaps (contact openings) to connect with the first side vertical contact (metalization 21). Later, metalization 31 is optionally provided, outside of the second gaps, to connect the pads 28 with indium bumps 30.

A bonding pad is not equivalent to a second metalization as recited as a bonding pad is a solid element that is arranged into the contact opening as opposed to particular liquid-to-solid processing for metalization. Further, metalization and bonding pads are distinctly described by Finnila (see FIG. 6; col. 5, lines 31-54).

Also, metalization 31, as disclosed by Finnila, makes no extension through the contact openings since it is positioned outside of the opening to connect the pad 28

(which does extend through the contact opening) with overglass layer 29 which is significantly different from a second metalization extending through a second gap as recited.

Again, the final rejection is premised on the erroneous observation of viewing the finished Finnila semiconductor device 1 (see FIG. 5) as a whole and noting its similarity with the present invention. This, of course, was apparently done without considering the critical, inventive steps towards vertically building up each particular layer of the integrated circuit. Such individually recited steps greatly differ from the steps taught or suggested by Finnila.

The final rejection fails to consider each individual step undertaken by the Finnila patent towards producing the semiconductor device, and comparing each individual step with the steps as recited towards producing a vertically integratable circuit. It is asserted that the Finnila patent fails to provide a bottomside metalization extending through a contact opening to connect with a topside metalization including circuit layers there connected.

Thus, the Finnila patent fails to disclose or suggest providing applying a second metalization along the second side of the first insulation layer, at least a portion of the second metalization extending through an at least one second gap to contact the first side vertical contact and defining a second side vertical contact as recited in claims 19-21, and equivalently recited in claim 23.

G. The Subject Matter Recited in Claims 19 and 23 is Not Anticipated by the Dekker Patent

In the discussion that follows, the appellants submit that the method of producing a vertically integratable circuit of claim 21, and the apparatus of claim 23 of the pending application, respectively, differ from the teachings of the Dekker patent. Specifically, Dekker fails to disclose applying a second metalization along the second side of the first insulation layer such that at least a portion of the second metalization extending through

an at least one second gap contacts the first side vertical contact and defines a second side vertical contact as recited.

In contrast to this recited feature of claim 19 (and equivalently recited in claim 23), Dekker expressly discloses providing conductive elements 20 within contact windows 19 on the bottomside of first insulating layer 3 to connect with source 9 of the transistor (see FIG. 6; col. 3, lines 66-67; col. 4, lines 1-11). However, Dekker expressly discloses that the contact windows 19 and conductive elements 20 therein are actually formed from the topside of the wafer 1 as opposed to forming the metalization along the second side (bottomside) of the first insulation layer as recited.

Due to the bottomside semiconductor material 18 blocking access to the first insulating material 3, Dekker forms all contact windows 12, 19 and conductive tracks 14, 20 from the topside (see FIGs. 4-6; col. 4, lines 2-11). After formation of all contact windows and conductive tracks from the topside, Dekker finally removes the bottomside substrate material 18 to allow connection of the contact wire 21 (see FIG. 6). In contrast, the claimed invention thins the bottomside (second) substrate allowing access to the first insulating material to form a second gap and apply a second metalization along the bottomside therein, extending through the second gap as recited.

Essentially, Dekker teaches that all components of the semiconductor device 1 which include bottom substrate 18, middle insulating layer 3, top substrate 4, insulating layer 11, electrical components 8, 9, 10, contact windows 12, 19, and conductive tracks 14, 20 must all be built up from the topside of the device 1, before removing the bottom substrate 18 to attach an external contact wire 21. In contrast, the present invention claims a vertically integratable circuit that provides first and second substrates, with a first insulation layer interposed between, where the second substrate is thinned allowing formation of a second gap and application of a second metalization along the bottomside of the first insulation layer. There is a significant difference between having to build up multiple semiconductor components all from the top side of the device as disclosed by Dekker as opposed to providing access to the bottomside of the first

insulation layer, by thinning the second substrate, to form a second gap and apply a second metalization layer therein.

Again, the final rejection is premised on the erroneous observation of viewing the finished Dekker semiconductor device 1 (see FIG. 6) as a whole and noting its similarity with the present invention, without considering the critical, inventive steps towards vertically building up each particular layer of the integrated circuit where these individual, recited steps greatly differ from the steps taught or suggested by Dekker. The final rejection fails to consider each individual step undertaken by the Dekker patent towards producing the semiconductor device, and comparing each individual step with the steps as recited towards producing a vertically integratable circuit. It is asserted that the Dekker patent fails to remove the bottomside substrate, exposing the first insulation layer, allowing formation of second gaps and application of metalization to the bottomside of the insulation layer.

Thus, the Dekker patent fails to disclose or suggest providing applying a second metalization along the second side of the first insulation layer, at least a portion of the second metalization extending through an at least one second gap to contact the first side vertical contact and defining a second side vertical contact as recited in claim 19, and equivalently recited in claim 23.

H. The Subject Matter Recited in Claim 20 is Not Made Obvious by the Combination of the Finnila and Livengood Patents

Livengood fails to make up for the above-described shortcomings of Finnila. Livengood is relied on only as a teaching of interrupting a second metalization at a first side vertical contact. Therefore, claim 20, being dependent from claim 19, is similarly distinguished from Livengood since Livengood omits the recited features of providing a first substrate with active circuit components along and within at least one portion thereof to define a first circuit layer, or applying a second insulation layer over a first circuit layer, and forming at least one first gap through the second insulation layer that

extends at least a portion into the first circuit layer and is in communication with the active circuit components thereof.

Thus, the Finnila and Livengood patents, either alone or in combination, fail to disclose or suggest applying a second metalization along the second side of the first insulation layer, at least a portion of the second metalization extending through an at least one second gap to contact the first side vertical contact and defining a second side vertical contact as recited in claim 20.

VIII. CONCLUSION

For the reasons set forth above, appended claims 19-21, and 23 of the pending application define subject matter that is not anticipated within the meaning of 35 U.S.C. § 102 over either the Finnila or Dekker patent, nor made obvious within the meaning of 35 U.S.C. § 103(a) over Finnila and Livengood.

The fee required by 37 C.F.R. § 1.17(c) is enclosed herewith.

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Respectfully submitted,

Date: February 9, 2005

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APPENDIX I

Claims on Appeal

Claims on Appeal

19. A method for making a vertically integratable circuit comprising the steps of:

providing first and second substrates, and a first insulation layer interposed between the first and second substrates, the first substrate located on a first side of the first insulation layer and the second substrate located on a second side of the first insulation layer opposed to the first side;

providing the first substrate with active circuit components along and within at least one portion thereof to define a first circuit layer;

applying a second insulation layer over the first circuit layer;

forming at least one first gap through the second insulation layer that extends at least a portion into the first circuit layer and is in communication with the active circuit components thereof;

filling the at least one first gap with a first metalization that defines at least one first side vertical contact;

thinning the second substrate to expose the second side of the first insulation layer;

forming at least one second gap through the first insulation layer that extends at least into a portion of the first circuit layer, the at least one second gap generally coinciding with the at least one first side vertical contact; and

applying a second metalization along the second side of the first insulation layer, at least a portion of the second metalization extending through the at least one second gap to contact the first side vertical contact and defining a second side vertical contact.

20. The method according to claim 19, wherein portions of the second metalization are interrupted at locations corresponding to the at least one first side vertical contact.

21. The method according to claim 19, wherein some of the active circuit components of the first circuit layer extend to the first insulation layer and surround

the connection between the first and second side vertical contacts.

23. A vertically integratable circuit, comprising:

a first insulation layer having a generally planar form, and opposed first and second sides, the first insulation layer defining at least one opening extending therethrough;

a first circuit layer bearing a plurality of active circuit components, a first side of the first circuit layer located on the first side of the first insulation layer;

a second insulation layer positioned on a second side of the first circuit layer opposed to the first side thereof, said second insulation layer having at least one first side vertical contact extending therethrough and into at least a portion of the first circuit layer; and

a second circuit layer located along the second side of the first circuit insulation layer and defined as a metallized layer, the second circuit layer having a second side portion extending through the at least one opening of the first insulation layer and into at least a portion of the first circuit layer so as to connect to the first side vertical contact.

APPENDIX III

Copy of Office Action of September 3, 2004

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09/926,377	12/13/2001	Thomas Grassl	GRAS3003/JEK	9840

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HOGANS, DAVID L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,377	GRASSL, THOMAS	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25 and 26* is/are allowed.

6)☒ Claim(s) *19-21 and 23* is/are rejected.

7)☐ Claim(s) *22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on June 30, 2004.

Status of Claims

Claims 19-26 are pending. Claims 1-18 are cancelled.

Claim Objections

1. Claims 24 and 26 are objected to because of the following informalities: Claim 24 line 3 and Claim 26 line 16, both refer to "the third metalization". Proper antecedent basis is lacking and appropriate correction is required.

Claim Rejections - 35 USC § 112

The previous rejections of Claims 11-18 under 35 U.S.C. § 112, first and second paragraphs, is withdrawn pursuant to the Amendments submitted by the Applicant on June 30, 2004.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 23 line 11 claims "a second circuit layer located along the second side of the first

circuit layer". The Examiner notes that the specification and disclosure teach the second circuit layer located along the second side of the first insulation layer.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. On page 6 of Applicant's remarks lines 18-19, support for Claim 21 is given. Applicant portends that active circuit components 8 extend around the connection between the first and second side vertical contacts 15 and 18. The Examiner notes that the area demarcated 8 is an oxide and not an active circuit.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 19, 21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,426,072 to Finnila.

In reference to Claim 19, Finnila teaches:

- providing first (12) and second (10) substrates, and a first insulation (11) layer interposed between the first and second substrates, the first substrate located on a first side of the first insulation layer and the second substrate located on a second side of the first insulation layer opposed to the first side; (See Figures 2-10 and columns 3-8 lines 01-10)

- providing the first substrate with active circuit components (transistors 18) along and within at least one portion thereof to define a first circuit layer; (See Figures 2-10 and columns 3-8 lines 01-10)
- applying a second insulation layer (20) over the first circuit layer; (See Figures 2-10 and columns 3-8 lines 01-10)
- forming at least one first gap (21) through the second insulation layer that extends at least a portion into the first circuit layer and is in communication with the active circuit components thereof; (See Figures 2-10 and columns 3-8 lines 01-10)
- filling the at least one first gap with a first metalization (21) that defines at least one first side vertical contact; (See Figures 2-10 and columns 3-8 lines 01-10)
- thinning the second substrate (10) to expose the second side of the first insulation (11) layer; (See Figures 2-10 and columns 3-8 lines 01-10)
- forming at least one second gap (28) through the first insulation layer that extends at least into a portion of the first circuit layer, the at least one second gap generally coinciding with the at least one first side vertical contact; (See Figures 2-10 and columns 3-8 lines 01-10) and
- applying a second metalization (28) along the second side of the first insulation layer, at least a portion of the second metalization extending through the at least one second gap to contact the first side vertical contact and defining a second side vertical contact (See Figures 2-10 and columns 3-8 lines 01-10)

In reference to Claim 21, Finnila teaches:

- wherein some of the active circuit components of the first circuit layer extend to the first insulation layer and surround the connection between the first and second side vertical contacts (See Figures 2-10 and columns 3-8 lines 01-10)

In reference to Claim 23, Finnila teaches:

- a first insulation layer having a generally planar form, and opposed first and second sides, the first insulation layer defining at least one opening extending therethrough; (See Figures 2-10 and columns 3-8 lines 01-10)
- a first circuit layer bearing a plurality of active circuit components, a first side of the first circuit layer located on the first side of the first insulation layer; (See Figures 2-10 and columns 3-8 lines 01-10)
- a second insulation layer positioned on a second side of the first circuit layer opposed to the first side thereof, said second insulation layer having at least one first side vertical contact extending therethrough and into at least a portion of the first circuit layer; (See Figures 2-10 and columns 3-8 lines 01-10) and
- a second circuit layer located along the second side of the first circuit layer and defined as a metallized layer, the second circuit layer having a second side portion extending through the at least one opening of the first insulation layer and into at least a portion of the first circuit layer so as to connect to the first side vertical contact (See Figures 2-10 and columns 3-8 lines 01-10)

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 19 and 23 rejected under 35 U.S.C. 102(e) as being anticipated by 6,104,081 to Dekker et al.

In reference to Claim 19, Dekker et al. teaches:

- providing first (4) and second substrates, and a first insulation (3) layer interposed between the first and second substrates, the first substrate located on a first side of the first insulation layer and the second substrate located on a second side of the first insulation layer opposed to the first side; (See Figures 1-6 and columns 3-5 lines 20-53)
- providing the first substrate with active circuit components (transistor 5) along and within at least one portion thereof to define a first circuit layer; (See Figures 1-6 and columns 3-5 lines 20-53)
- applying a second insulation layer (11) over the first circuit layer; (See Figures 1-6 and columns 3-5 lines 20-53)
- forming at least one first gap (12) through the second insulation layer that extends at least a portion into the first circuit layer and is in communication with

the active circuit components thereof; (See Figures 1-6 and columns 3-5 lines 20-53)

- filling the at least one first gap with a first metalization (14) that defines at least one first side vertical contact; (See Figures 1-6 and columns 3-5 lines 20-53)
- thinning the second substrate to expose the second side of the first insulation (3) layer; (See Figures 1-6 and columns 3-5 lines 20-53)
- forming at least one second gap (19) through the first insulation layer that extends at least into a portion of the first circuit layer, the at least one second gap generally coinciding with the at least one first side vertical contact; (See Figures 1-6 and columns 3-5 lines 20-53) and
- applying a second metalization (21) along the second side of the first insulation layer, at least a portion of the second metalization extending through the at least one second gap to contact the first side vertical contact and defining a second side vertical contact (See Figures 1-6 and columns 3-5 lines 20-53)

In reference to Claim 23, Dekker et al. teaches:

- a first insulation layer having a generally planar form, and opposed first and second sides, the first insulation layer defining at least one opening extending therethrough; (See Figures 1-6 and columns 3-5 lines 20-53)
- a first circuit layer bearing a plurality of active circuit components, a first side of the first circuit layer located on the first side of the first insulation layer; (See Figures 1-6 and columns 3-5 lines 20-53)

- a second insulation layer positioned on a second side of the first circuit layer opposed to the first side thereof, said second insulation layer having at least one first side vertical contact extending therethrough and into at least a portion of the first circuit layer; (See Figures 1-6 and columns 3-5 lines 20-53) and
- a second circuit layer located along the second side of the first circuit layer and defined as a metallized layer, the second circuit layer having a second side portion extending through the at least one opening of the first insulation layer and into at least a portion of the first circuit layer so as to connect to the first side vertical contact (See Figures 1-6 and columns 3-5 lines 20-53)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,426,072 to Finnila in view of 6,495,454 to Livengood et al.

Incorporating all arguments of Claim 19 and noting that Finnila fails to explicitly teach wherein portions of the second metalization are interrupted at locations corresponding to the at least one first side vertical contact.

However, Livengood et al., in Figures 3 and 4 and columns 6-7 lines 10-56, teaches wherein portions of the second metalization (326 or 410) are interrupted at locations corresponding to the at least one first side vertical contact (316, 318 or 421b).

It would have been obvious to one of ordinary skill in the art to modify Finnila by incorporating wherein portions of the second metalization are interrupted at locations corresponding to the at least one first side vertical contact, as taught by Livengood et al., to different interconnects within an integrated circuit.

Allowable Subject Matter

6. Claims 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 25 and 26 are allowable.

8. The following is a statement of reasons for the indication of allowable subject matter.

The prior art of record fails to teach or suggest, in combination with the other claimed features, an annular metalization extending through the second insulation layer and into at least a portion of the first circuit layer, the third metalization annularly surrounding the first side vertical contact with at least a portion of the active circuit components interposed therebetween.

Response to Arguments

9. Applicant's arguments with respect to newly submitted claims 19-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (571) 272-1691. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DH

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
09/926,377	GRASSL, THOMAS	
Examiner	Art Unit	Page 1 of 1
David L. Hogans	2813	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,495,454	12-2002	Livengood et al.	438/667
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.